S.E. Computer (III) (CBGS). 9/12/15

DLDA

QP Code : 5211

Instructions for the students: **(3 Hours)** **[Total Marks : 80**

1) Question number 1 is compulsory.
2) Attempt any 3 questions from the remaining 5 questions.
3) Each question carries 20 marks.

Q1(a): Convert decimal number 199.375 into binary, octal, hexadecimal system.

(b): Perform hexadecimal arithmetic operation: DADA + BABA.

(c): Convert binary data 1010 into 7 bit even parity hamming code.

(d): Express the equation in standard POS form: F (A, B, C) = Σ m (0, 2, 5,7).

(e): Differentiate in brief between combinational & sequential circuits.

(f): Compare TTL & CMOS with respect to speed, power dissipation, fan-in & fan-out.

(g): Explain in brief weighted & non-weighted codes with one exampie each.

(h): Explain the race around condition in JK flip-flop. State various methods to overcome it.

(i): Convert JK flip-flop into D-flip-flop & T-flip-flop (show only the design without steps).

(j): What is Modulus of the counter? For MOD-6 counter how many flip-flops are needed?

Q2(a): Simplify the following equation using K-map to obtain minimum POS equation & realize the minimum equation using only NOR gates.

F (A, B, C, D) = Σ m (1, 3, 4, 6, 9, 11, 12, 14)

(b): What is Multiplexer tree? Construct 32:1 multiplexer using 8:1 multiplexers only. Explain how the logic on particular data line is steered to the output in this design with example.

Q3(a): Reduce using Quine McClusky method & realize the equation using only NAND gates.

F(P, Q, R, S) = Σ m (0, 1, 2, 8, 10, 11, 14, 15)

(b): Implement single digit BCD adder using 4-bit binary adder IC 7483. Show the design procedure & explain its operation.

Q4 (a): Explain the concept of comparator. Develop the truth table for 2-bit binary comparator & design it using a suitable decoder & additional gates.

(b): Design MOD-5 synchronous up-counter using JK flip-flops with all the design steps.

Q5 (a): Input to a combinational circuit is a 4-bit binary number. Design the circuit with minimum hardware for the following:

- Output P = 1 if the number is prime.
- Output Q = 1 if the number is divisible by 3.

(b): Draw a circuit diagram for 3-bit asynchronous binary down counter using master-slave JK flip-flops. Show the output of each flip-flop with reference to the clock & justify that the down counting action. Also prove from the timing diagram that the counter is "divide by 8" counter.

Q6 (a): What is shift register? Explain 4-bit bidirectional shift register.

(b): Draw & explain the working of 4-bit ring counter with timing diagram.

MD-Con. 10469-15.
